14.4 A 380MHz, 150mW Direct Digital Synthesizer/Mixer in 0.25μm CMOS

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A Direct Digital Frequency Synthesizer/Mixer (DDFSM) is an useful building-block in many communication subsystems such us tuners, derotators, up and down frequency converters, etc. The inputs of a DDFSM are two signals *Xin* and *Yin*, and a frequency control word *f*. The outputs are computed as follows:

$$Xout(n)=Xin(n)\cos(2\pi f\,n)-Yin(n)\sin(2\pi f\,n);$$
$$Yout(n)=Xin(n)\sin(2\pi f\,n)+Yin(n)\cos(2\pi f\,n).$$

The simplest DDFSM implementation includes a Direct-Digital Frequency Synthesizer (DDFS) to generate the sequences: $\sin(2\pi f\,n)$ and $\cos(2\pi f\,n)$ feeding a complex multiplier (mixer). Another common approach uses a phase accumulator driving a CORDIC rotator. Both approaches are non-optimal in terms of hardware resources, and improved techniques using the cascade of two "coarse" and "fine" rotation stages have been recently proposed [1,2].

The top-level architecture of the designed DDFSM IC is shown in Fig. 14.4.1. The circuit exhibits 90dBc Spurious Free Dynamic Range (SFDR). The input word-length is 12b while output word-length is 13b. The phase accumulator, truncated to 16b, generates the rotation angle. The heart of the circuit is the *Hybrid CORDIC rotator*, which is able to perform a rotation by an angle φ in [0,π/4], represented as a binary fraction with 13b. The other minor subsystems in Fig. 14.4.1 (1's complementer, swappers and 2's complementers controlled by a decode logic) employ the sine and cosine functions symmetries [1,2] to perform the complete rotation in the full [0,2π] interval.

The *Hybrid CORDIC rotator* subdivides the rotation in three steps (see Fig. 14.4.2). To that purpose, the angle φ is partitioned as: $\varphi=\alpha+\beta$, where α includes the three Most Significant Bits (MSBs) of α, while β includes the remaining 10 bits of φ.

In the first rotation block of Fig. 14.4.2 we used a modified CORDIC datapath to perform a coarse rotation by an angle close to α. The rotation directions are computed in parallel, by using a small lookup table, in order to avoid the delay of the angle computation block. To reduce the hardware further, only four rotation stages are employed, resulting in a rotation by an angle $\alpha'\neq\alpha$. The residual angle, $Z_{residual}=\alpha'-\alpha'$ can be precomputed and stored in the lookup table, as shown in Fig. 14.4.2. The remaining rotation angle after the first stage is computed as $\gamma=\beta+Z_{residual}$, by using the π/4 multiplier (needed to calculate β from its scaled representation) and the adder shown in Fig. 14.4.2. The angle γ is computed with 11 bits of accuracy in Fig. 14.4.2 and partitioned as: $\gamma=\gamma_1+\gamma_2$, where γ_1 includes the three MSBs of γ, while γ_2 includes the remaining 8 bits.

The second rotation block in Fig. 14.4.2 performs the rotation by γ_1. This stage is also CORDIC based. However, since γ_1 is a small angle, the bits of γ_1 can be used directly to drive the rotation directions of the second CORDIC rotation, with a negligible error.

The third rotation block in Fig. 14.4.2 implements the final rotation by γ_2. This step could also be computed by using CORDIC. However, we used a complex multiplier to reduce latency and improve performance. Since γ_2 is small, a first-order Taylor approximation of sine and cosine functions is employed: $\sin(\gamma_2)\cong\gamma_2$, $\cos(\gamma_2)\cong 1$. In this way two multipliers are needed for the third rotation, as shown in Fig. 14.4.2, without the need of look-up tables to store the values of trigonometric functions. The inputs of the two multipliers are appropriately rounded, to reduce the partial products while maintaining the output error below a desired threshold. The sizing in Fig. 14.4.2 allows the circuit to reach more than 90dBc SFDR, while minimizing the silicon area.

Since the CORDIC rotation directions are efficiently evaluated in parallel, the implementation of the CORDIC stages was performed by using Carry Save arithmetic. Indicating with σ, the direction of the CORDIC rotation ($\sigma=\pm 1$), the operation to be performed in CarrySave is:

$$O^S + O^C = X^S + X^C - \sigma\cdot 2^{-i}\cdot Y^S - \sigma\cdot 2^{-i}\cdot Y^C$$

The basic building block to implement the above equation includes a 4–2 compressor, with two XORs to conditionally complement the shifted Y^S and Y^C values, as shown in Fig. 14.4.3. This figure also reports an optimized gate-level implementation that we have obtained, with only three gates on the critical path.

In order to simplify the IC design, the DDFSM has been implemented by using a standard cell approach. To optimize performance, special purpose cells were designed implementing the circuit in Fig. 14.4.3 (and other timing-critical circuits) with Double-Pass-Transistor logic (DPL) [3], see Fig. 14.4.4. DPL is a double rail logic. In the developed cells, each input is converted from single to dual rail by using a couple of inverters. In this way pass-gate inputs, that are not suited for the timing models used by the timing analysis tools, are also avoided. The inverters in the circuit of Fig. 14.4.4 increase the circuit speed by limiting the maximum number of series transistors. Moreover, they make the propagation delay of the *Carry* output independent from the capacitive load on the *Sum* output, and vice versa. In this way the developed DPL circuits are fully compatible with the other full-CMOS standard cells of the library, and a design style which joins DPL and CMOS cells can easily be implemented. For comparison, we implemented the circuits in Fig. 14.4.3 with and without DPL cells. The use of DPL cells allowed a reduction in the stage delay from 1.03ns to 0.76ns, with the same power dissipation and silicon area.

A DDFSM IC has been fabricated on a test chip in TSMC 0.25μm, 2.5V CMOS technology (see Fig. 14.4.7). The chip includes a built-in self-test structure to facilitate the experimental measurement of the maximum clock frequency and power dissipation. The circuit accepts a 32b frequency control word, resulting in a tuning resolution of about 0.088Hz. Figure 14.4.5 reports the output spectrum of the chip operating in DDS mode (*Xin*=1; *Yin*=0), showing an SFDR larger than 93dBc.

Figure 14.4.6 summarizes the experimental performance of the DDFSM, along with the best designs available today [1,2] implemented with the same technology. A more than three-fold reduction of power dissipation is shown. With respect to [2], that reaches 100dBc SFDR, a two-fold reduction of silicon area is shown. The clock frequency also compares favorably with [1] and [2].

Acknowledgements:
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References:
[1] A. Torosyan, D. Fu, A. N. Wilson, "A 300 MHz direct digital synthesizer/mixer in 0.25 μm CMOS," *IEEE J. Solid-State Circuits*, vol. 38, no. 6, pp. 875–887, June, 2003.
[2] Y. Song, B. Kim, "A quadrature digital synthesizer/mixer architecture using fine/coarse coordinate rotation to achieve 14-b input, 15-b output, and 100-dBc SFDR," *IEEE J. Solid-State Circuits*, vol. 39, no. 11, pp. 1853-1861, Nov., 2004.
[3] M. Suzuki et al: "A 1.5 ns 32 b CMOS ALU in Double Pass-Transistor Logic," *IEEE J. Solid State Circuits*, vol. 28, no. 11, pp. 1145-1151, Nov., 1993.

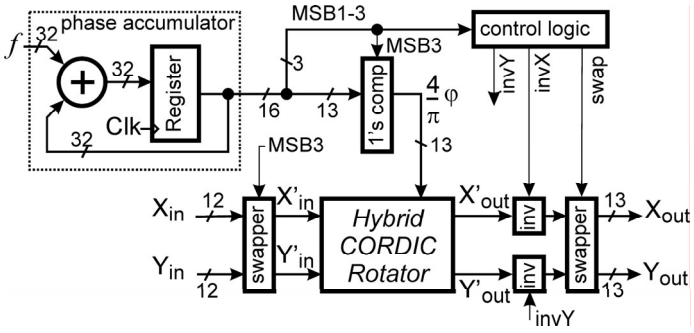

Figure 14.4.1: Direct digital synthesizer/mixer architecture.

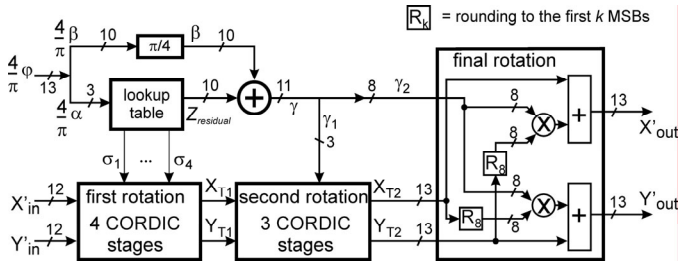

Figure 14.4.2: Hybrid-CORDIC rotator.

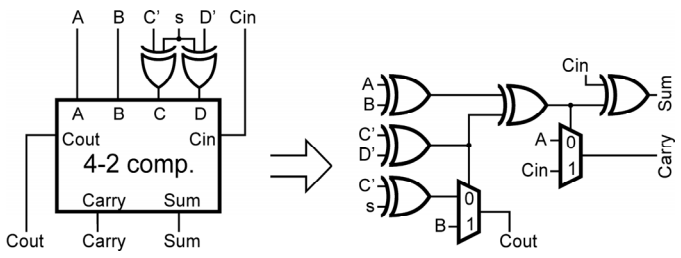

Figure 14.4.3: Basic building block for the realization of the CORDIC rotation and its gate level implementation with 3 gates on the critical path.

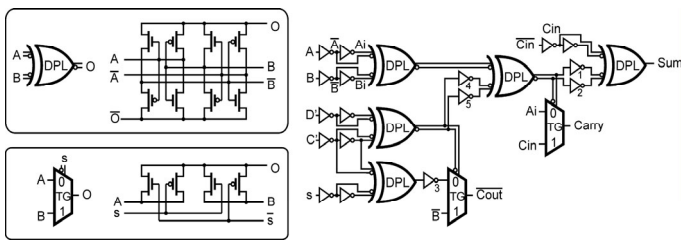

Figure 14.4.4: Implementation of the circuit of Fig. 14.4.3 in DPL.

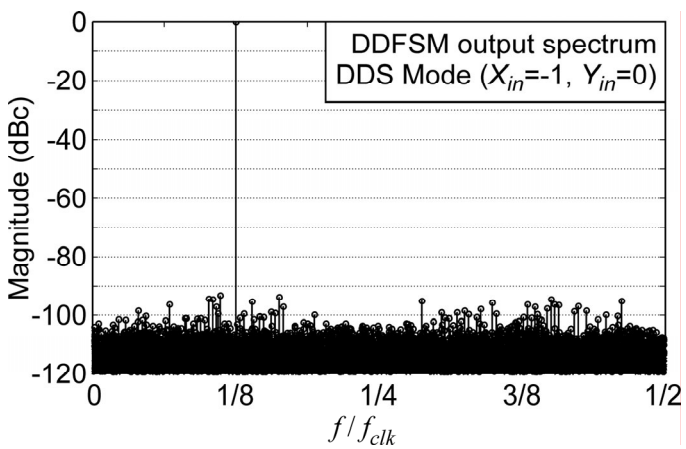

Figure 14.4.5: Output spectrum of the DDFSM in DDS mode (X_{in}=-1, Y_{in}=0).

Circuit	Technique	Accum. (bits)	SFDR (dBc)	Input (bits)	Output (bits)	Process (μm)	Area (mm^2)	Data Rate (MHz)	P_D (mW/MHz)
This paper	Hybrid-CORDIC	32	90	12	13	0.25	0.22	385	0.40
Torosyan [1] ***JSSC 2003***	Two stages mult-based	32	90	12	13	0.25	0.36	300	1.33
Song [2] ***JSSC 2004***	Two stages mult-based	32	100	14	15	0.25	0.51	330	1.39

Figure 14.4.6: Experimental performance of the proposed DDFSM IC and comparison with recently proposed designs.

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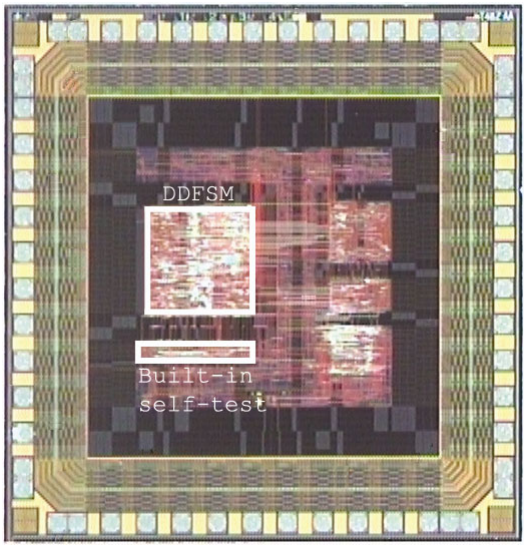

Figure 14.4.7: Test chip micrograph.

